SPECIFICATION AMENDMENTS:

Please amend the paragraph beginning at page 5, line ~~20~~ 21 as follows:

"Referring to FIGS. 2A and 2B, a testcase 150 and a microprocessor 110 in accordance with an instruction set architecture of the present invention is shown. Testcase 150 includes operating instructions 160, a triggering instruction 170, a triggering instruction 171, and a triggering instruction 172. Operating instructions 160 is for operating a processor core 120 of microprocessor 110. Triggering instruction 170 is for transitioning a debugging unit 130 of microprocessor 110 to a base operating state. Triggering instruction 171 is for transitioning debugging unit 130 to an operating state whereby trace array 131 dynamically stores trace data TRD from a processor core 120 of microprocessor 110 (hereinafter "the dynamic storing operating state"). Triggering instruction 172 is for transitioning debugging unit 130 to an operating state whereby trace array 131 statically stores trace data TRD (hereinafter "the static storage operating state"). Triggering instruction 170, triggering instruction 171, and triggering instruction 172 are strategically embedded within operating instructions 160 to sequentially transition debugging unit 130 between the base operating state, the dynamic storage operating state, and the static storage operating state."

Please amend the paragraph beginning at page 6, line ~~12~~ 27 as follows:

"Processor core 120 provides a register address signal RA_{S2} to register 123 in response to trigger instruction signal TI_{S2}. Register 123 provides trigger event signal TE_{S2} (~~FIG. 2~~ FIG. 1) to debugging unit 130 in response to register address signal RA_{S2}. Logic analyzer 132 transitions debugging unit 130 to the dynamic storage operating state in response trigger event signal TE_{S2}. Specifically, logic analyzer 132 provides a write enable signal WE_S to trace array 131 in response to trigger event signal TE_{S2}. Trace array 131 dynamically store trace data TRD in response to write enable signal WE_S."

Please amend the paragraph beginning at page ~~6~~ 7, line ~~20~~ 3 as follows:

"Processor core 120 provides a register address signal RA_{S3} to register 124 in response to trigger instruction signal TI_{S3}. Register 124 provides trigger event signal TE_{S3} (FIG. 1) to debugging unit 130 in response to register address signal RA_{S3}. Logic analyzer 132 transitions debugging unit 130 to the static storage operating state in response trigger event signal TE_{S2} $\underline{TE_{S3}}$. Specifically, logic analyzer 132 ceases any provision of write enable signal WE_S to trace array 131 in response to trigger event signal TE_{S3}. Trace array 131 statically stores any trace data TRD written into trace array 131 during the ~~dynamic~~ static storage operating state."

Please amend the paragraph beginning at page 7, line ~~10~~ 23 as follows:

"Referring to FIGS. 3A and 3B, a testcase 151 and a microprocessor 111 in accordance with an instruction set architecture of the present invention is shown. Testcase 151 includes operating instructions 160 (FIG. 2A), triggering instruction 170 (FIG. 2A), a set of operating instructions 173, triggering instruction 171 (FIG. 2A), and triggering instruction 172 (FIG. 2A). Operating instructions 173 are for generating trigger data or non-event data. Triggering instruction 170 and triggering instruction 172 are strategically embedded within operating instructions 160 to transition debugging unit 130 to the base operating state and the static storage operating state, respectively. Operating instructions 173 and triggering instruction ~~172~~ 171 are sequentially and strategically embedded within operating instructions 160 to optionally transition debugging unit 130 to the dynamic storage operating state."

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Please amend the paragraph beginning at page 8, line ~~11~~ as follows:

"In response to data instruction signals DI_{S1}, processor core 120 provides either a trigger data signal TD_{S1} to register 25 when processor core 120 generates trigger data, or provides a non-event data signal ND_{S1} to register 25 when processor core 120 generates the non-event data. For example, processor core 120 can perform a XOR operation of two general purpose registers (not shown) in response to data instruction signals DI_{S1}. The contents of one ~~registers~~ register can be a pre-defined constant. The contents of the other register can be a testcase number for test case 151 that matches the pre-defined constant, or any other number. Trigger data can be defined as the result of a match of the pre-defined constant and the testcase number for testcase 151, i.e. the XOR operation yielding all zeros. Non-event data can be defined as the results of a mismatch of the pre-defined constant and any other number, i.e. the XOR operation yielding some ones."

13

Please amend the paragraph beginning at page 9, line ~~7~~ as follows:

"Processor core 120 provides register address signal RA_{S3} to register 124 in response to trigger instruction signal TI_{S3}. Register 124 provides trigger event signal TE_{S3} (FIG. 1) to debugging unit 130 in response to register address signal RA_{S3}. Logic analyzer 132 transitions debugging unit 130 to the static storage operating state in response trigger event signal ~~TE_{S2}~~ TE_{S3}."

Please amend the paragraph beginning at page 9, line 8 as follows:

"It is to be appreciated that the processing of trigger instruction signal TI_{S1}, data instruction signals DI_{S1}, trigger instruction signal TI_{S2}, and trigger instruction signal TI_{S3} by processor core 120 transitions debugging unit 130 to the base operating state and the static storage operating state, and selectively ~~transition~~ transitions debugging unit 130 to the dynamic storage operating state. Consequently, upon the completion of processing instruction stream IS_2 by processor core 120, any trace data TRD stored within trace array 131 is representative of the results of processing testcase 151 by processor core 120."

29

Please amend the paragraph beginning at page 9, line ~~17~~ as follows:

"Referring to FIGS. 4A and 4B, a testcase 152 and a microprocessor 112 in accordance with an instruction set architecture of the present invention is shown. Testcase 152 includes operating instructions 160 (FIG. 2A), triggering instruction 170 (FIG. 2A), a set of operating instructions 174, triggering instruction 171 (FIG. 2A), and triggering instruction 172 (FIG. 2A). Operating instructions 174 are to generate a first trigger data or a second trigger data. Triggering instruction 170 and triggering instruction 172 are strategically embedded within operating instructions 160 to transition debugging unit 130 to the base operating state and the static storage operating state, respectively. Operating instructions 174 and triggering instruction ~~172~~ 171 are sequentially and strategically embedded within operating instructions 160 to selectively transition debugging unit 130 to the dynamic storage operating state or the base operating state."

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Please amend the paragraph beginning at page 11, line ~~1~~ as follows:

"Processor core 120 provides register address signal RA_{S3} to register 124 in response to trigger instruction signal TI_{S3}. Register 124 provides trigger event signal TE_{S3} (FIG. 1) to debugging unit 130 in response to register address signal RA_{S3}. Logic analyzer 132 transitions debugging unit 130 to the static storage operating state in response trigger event signal ~~TE_{S2}~~ TE_{S3}."

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Please amend the paragraph beginning at page 11, line ~~1~~ as follows:

"It is to be appreciated that the processing of trigger instruction signal TI_{S1}, data instruction signal DI_{S2}, trigger instruction $T1_{S3}$, and trigger instruction signal TI_{S3}~~, trigger instruction signal TI_{S6}, and trigger instruction signal TI_{S7}~~ by processor core 120 transitions debugging unit 130 to the base operating state and the static storage operating state, and selectively transition debugging unit 130 to either the dynamic storage operating state or the base operating state. Consequently, upon the completion of processing instruction stream IS_3 by processor core 120, any trace data TRD stored within trace array 131 is representative of the results of processing testcase 152 by processor core 120."

17

Please amend the paragraph beginning at page 11, line ~~16~~ as follows:

"From the previous descriptions of the present invention in connection with FIGS. 2A-4B, one skilled in the art will know how to make and use other embodiments of test cases and microprocessors in accordance with the present invention. For example, one skilled in the art will know how to make and use a test case including one or more triggering instructions 170 (FIG. 2A); one or more triggering instructions 171 (FIG. 2A); one or more triggering instructions 172 (FIG. 2A); one or more sets of operating instructions 173 (FIG. 3A); and/or one or more sets of operating instructions 174 (FIG. 4A). Also by example, one skilled in the art will know how to make and use a microprocessor including one or more registers 122 (FIG. 2B); one or more registers 123 (FIG. 2B); one or more registers 124 (FIG. 2B); one or more registers 125 (FIG. 3B); and/or one or more registers 126 (FIG. ~~3B~~ 4B)."

Please delete the Abstract of the invention in its entirety, and add the following new Abstract as attached hereto.